

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * CU12 cross page boundary instruction tests
				5 *
				6 * NOTE: This test is based the CLCL-et-al Test
				7 * modified to only test the CU12 instruction.
				8 *
				9 * James Wekel February 2024
				10 *****
				12 *****
				13 *
				14 * CU12 cross page instruction tests
				15 *
				16 *****
				17 * This program tests functioning of the CU12 instruction
				18 * across page boundaties. Only MB=0 is tested and CC=0 is expected.
				19 * Specification exceptions are not tested.
				20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				22 * obvious coding errors. None of the tests are thorough. They are
				23 * NOT designed to test all aspects of any of the instructions.
				24 *
				25 *****
				26 *
				27 * Example Hercules Testcase:
				28 *
				29 * *Testcase CU12-01-xpage (Test cross page CU12 instruction)
				30 *
				31 * # -----
				32 * # This tests only the function of the CU12 instruction where
				33 * # operands cross page boundaries.
				34 * # Specification Exceptions are NOT tested.
				35 * # -----
				36 *
				37 * main size 16
				38 * numcpu 1
				39 * sysclear
				40 * archlvl z/Arch
				41 *
				42 * loadcore "\$(testpath)/CU12-01-xpage.core" 0x0
				43 *
				44 * runtest 1
				45 *
				46 * *Done
				47 *
				48 *****

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT				
00000000			00000000 00000000	000006BB	50 51	CU12TST	START 0 USING	CU12TST, R0	Low core addressability
00000000 000001A0 000001A8			00000000	000001A0	53 54 55		ORG DC DC	CU12TST+X' 1A0' X' 00000000180000000' AD(BEGIN)	z/Architecure RESTART PSW
000001B0 000001D0 000001D8			000001B0	000001D0	57 58 59		ORG DC DC	CU12TST+X' 1D0' X' 0002000180000000' AD(X' DEAD')	z/Architecure PROGRAM CHECK PSW
000001E0			000001E0	00000200	61		ORG	CU12TST+X' 200'	Start of actual test program ..
					63	*****			
					64	* The actual "CU12TST" program itself...			
					65	*****			
					66	*			
					67	* Architecture Mode: z/Arch			
					68	* Register Usage:			
					69	*			
					70	* R0 interation count for current test			
					71	* R1 current target address			
					72	* R2 CU12 - First-Operand Address - target			
					73	* R3 CU12 - First-Operand Length			
					74	* R4 CU12 - Second-Operand Address - source			
					75	* R5 CU12 - Second-Operand length			
					76	* R6 (work)			
					77	* R7 CU12CTL base			
					78	* R8 First base register			
					79	* R9 Second base register			
					80	* R10-R13 (work) (copy source)			
					81	* R14 Subroutine call			
					82	* R15 Secondary Subroutine call or current source address			
					83	*			
					84	*****			
00000200 00000200			00000200 00001200		86 87		USING USING	BEGIN, R8 BEGIN+4096, R9	FIRST Base Register SECOND Base Register
00000200 00000202 00000204	0580 0680 0680				89 90 91	BEGIN	BALR BCTR BCTR	R8, 0 R8, 0 R8, 0	Initalize FIRST base register Initalize FIRST base register Initalize FIRST base register
00000206 0000020A	4190 8800 4190 9800			00000800 00000800	93 94		LA LA	R9, 2048(, R8) R9, 2048(, R9)	Initalize SECOND base register Initalize SECOND base register
					95	*			
					96	** Run the tests...			
					97	*			
0000020E	45E0 8302			00000502	98 99		BAL	R14, TEST01	Test CU12 instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				125	*****		
				126	*	TEST01	Test CU12 instruction
				127	*****		
00000502	9201 8200		00000400	129	TEST01	MVI	TESTNUM, X' 01'
				130			
00000506	4170 83F8		000005F8	131		LA	R7, CU12CTL
0000050A		00000000		132		USING	CU12TEST, R7
				133			Point R7 --> testing control table What each table entry looks like
		0000050A	00000001	134	TST1LOOP	EQU	*
0000050A	4360 7000		00000000	135		IC	R6, TNUM
0000050E	4260 8200		00000400	136		STC	R6, TESTNUM
				137			Set test number
00000512	5800 7010		00000010	138		L	R0, OP2LEN
				139	*		source length
00000516	58F0 7014		00000014	140		L	R15, OP1WHERE
0000051A	1BF0			141		SR	R15, R0
0000051C	41F0 F001		00000001	142		LA	R15, 1(, R15)
				143	*		Calculate Target address
00000520	5810 7018		00000018	144		L	R1, OP2WHERE
00000524	1B10			145		SR	R1, R0
00000526	4110 1001		00000001	146		LA	R1, 1(, R1)
				147	*		Calculate source address
				148	**		Initialize source operand data (move data to testing address)
				149	*		
		0000052A	00000001	150	TST1INIT	EQU	*
				151	*		Source
0000052A	18A1			152		LR	R10, R1
0000052C	58B0 7010		00000010	153		L	R11, OP2LEN
00000530	58C0 700C		0000000C	154		L	R12, OP2DATA
00000534	58D0 7010		00000010	155		L	R13, OP2LEN
00000538	0EAC			156		MWCL	R10, R12
				157			
				159	*		Execute CU12 instruction and check for expected condition code
0000053A	182F			161		LR	R2, R15
0000053C	5830 7008		00000008	162		L	R3, OP1LEN
00000540	1841			163		LR	R4, R1
00000542	5850 7010		00000010	164		L	R5, OP2LEN
				165			target target length source source length
00000546	1B66			166		SR	R6, R6
00000548	4360 7003		00000003	167		IC	R6, MB
0000054C	4260 835E		0000055E	168		STC	R6, CU12MDD+2
				169			get MB bits for CU12 (MB) DYNAMICALLY MODIFIED CODE
00000550	58B0 701C		0000001C	170		L	R11, FAILMASK
00000554	89B0 0004		00000004	171		SLL	R11, 4
				172			(failure CC) (shift to BC instr CC position)
00000558	9200 8201		00000401	173		MVI	SUBTEST, X' 00'
0000055C	B2A7 0024			174	CU12MDD	CU12	(primary CU12) Start with CU12 and mB=0
00000560	4710 835C		0000055C	175		BC	B' 0001', CU12MDD
				176			cc=3, not finished
00000564	44B0 83C4		000005C4	177		EX	R11, CU12BC
							fail if...

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				219	*****
				220	* Normal completion or Abnormal termination PSWs
				221	*****
000005C8	00020001 80000000			223	E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
000005D8	B2B2 83C8		000005C8	225	E0J LPSWE E0JPSW Normal completion
000005E0	00020001 80000000			227	FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
000005F0	B2B2 83E0		000005E0	229	FAILTEST LPSWE FAILPSW Abnormal termination
				231	*****
				232	* Working Storage
				233	*****
000005F4				235	LTORG , Literals pool
000005F4	00000000			236	=F' 0'
	00000400	00000001		238	K EQU 1024 One KB
	00001000	00000001		239	PAGE EQU (4*K) Size of one page
	00004000	00000001		240	K16 EQU (16*K) 16 KB
	00008000	00000001		241	K32 EQU (32*K) 32 KB
	00010000	00000001		242	K64 EQU (64*K) 64 KB
	00100000	00000001		243	MB EQU (K*K) 1 MB

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				307	*****
				308	* CU12 UTF-8 tests
				309	*****
0000062C	0000003D			311	UTF8ALN DC A(UTF8AEND- UTF8A)
00000630				312	UTF8A DS 0H
00000630	00			313	DC XL1' 00' first UTF-8 1 Byte character
00000631	31			314	DC XL1' 31' 1
00000632	39			315	DC XL1' 39' 9
00000633	40			316	DC XL1' 40' @
00000634	41			317	DC XL1' 41' A
00000635	42			318	DC XL1' 42' B
00000636	7F			319	DC XL1' 7F' last UTF-8 1 Byte character
00000637	C280			321	DC XL2' C280' first UTF-8 2 Byte character
00000639	C380			322	DC XL2' C380' c3 80 LATIN CAPITAL LETTER A WITH GRAVE
0000063B	C3B8			323	DC XL2' C3B8' c3 b8 LATIN SMALL LETTER O WITH STROKE
0000063D	D09C			324	DC XL2' D09C' D0 9C Dœ Cyrillic Capital Letter Em
0000063F	DFBF			325	DC XL2' DFBF' last UTF-8 2 Byte character DF BF БҀ
00000641	43			327	DC XL1' 43' C
00000642	E0A080			329	DC XL3' E0A080' first UTF-8 3 Byte character
				330	* E0 A0 80 à € Samaritan Letter Alaf
00000645	E0A18D			331	DC XL3' E0A18D' E0 A1 8D à• Mandaic Letter An
00000648	EA9FBD			332	DC XL3' EA9FBD' EA 9F BD êŸ½ Latin Epigraphic Inverted M
0000064B	EFBF87			333	DC XL3' EFBF87' EF BF 87 ïꞤ Halfwidth Hangul Letter E
0000064E	EFBFBF			334	DC XL3' EFBFBF' last UTF-8 3 Byte character EF BF БҀ
00000651	44			336	DC XL1' 44' D
00000652	F0908080			338	DC XL4' F0908080' first UTF-8 4 Byte character
				339	* F0 90 80 80 ð•€€ Linear B Syllable B008 A
00000656	F0908487			340	DC XL4' F0908487' F0 90 84 87 ð•,Ꞥ Aegean Number One
0000065A	F09294B5			341	DC XL4' F09294B5' F0 92 94 B5 Cuneiform Sign She Plus Sar
0000065E	F09082B8			342	DC XL4' F09082B8' F0 90 82 B8 ð•, Linear B Ideogram B177
00000662	F096AB83			343	DC XL4' F096AB83' F0 96 A8 83 ð-Ꞥ Bamum Letter Phase-f Ka
00000666	F0989A9F			344	DC XL4' F0989A9F' last UTF-8 4 Byte character
0000066A	45			346	DC XL1' 45' E
0000066B	4E			347	DC XL1' 4E' N
0000066C	44			348	DC XL1' 44' D
0000066D				349	UTF8AEND DS 0X
				350	
				352	*****
				353	* CU12 UTF-12 Result
				354	*****
0000066D	E4C6E3F3 F27A			355	DC C' UFT32: '
00000674	00000044			356	UTF16ALN DC A(UTF16AED- UTF16A)
00000678				357	UTF16A DC 0X
00000678	0000			358	DC X' 0000'
0000067A	0031			359	DC X' 0031'
0000067C	0039			360	DC X' 0039'
0000067E	0040			361	DC X' 0040'
00000680	0041			362	DC X' 0041'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00000682	0042			363	DC	X' 0042'
00000684	007F			364	DC	X' 007F'
00000686	0080			365	DC	X' 0080'
00000688	00C0			366	DC	X' 00C0'
0000068A	00F8			367	DC	X' 00F8'
0000068C	041C			368	DC	X' 041C'
0000068E	07FF			369	DC	X' 07FF'
00000690	0043			370	DC	X' 0043'
00000692	0800			371	DC	X' 0800'
00000694	084D			372	DC	X' 084D'
00000696	A7FD			373	DC	X' A7FD'
00000698	FFC7			374	DC	X' FFC7'
0000069A	FFFF			375	DC	X' FFFF'
0000069C	0044			376	DC	X' 0044'
				377	*	
0000069E	D800			378	DC	X' D800'
000006A0	DC00			379	DC	X' DC00'
000006A2	D800			380	DC	X' D800'
000006A4	DD07			381	DC	X' DD07'
000006A6	D809			382	DC	X' D809'
000006A8	DD35			383	DC	X' DD35'
000006AA	D800			384	DC	X' D800'
000006AC	DCB8			385	DC	X' DCB8'
000006AE	D81A			386	DC	X' D81A'
000006B0	DEC3			387	DC	X' DEC3'
000006B2	D821			388	DC	X' D821'
000006B4	DE9F			389	DC	X' DE9F'
				390		
000006B6	0045			391	DC	X' 0045'
000006B8	004E			392	DC	X' 004E'
000006BA	0044			393	DC	X' 0044'
000006BC				394	UTF16AED DS	0X

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
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396 ****
397 *      Register equates
398 ****

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00000000	00000001	400	R0	EQU	0
00000001	00000001	401	R1	EQU	1
00000002	00000001	402	R2	EQU	2
00000003	00000001	403	R3	EQU	3
00000004	00000001	404	R4	EQU	4
00000005	00000001	405	R5	EQU	5
00000006	00000001	406	R6	EQU	6
00000007	00000001	407	R7	EQU	7
00000008	00000001	408	R8	EQU	8
00000009	00000001	409	R9	EQU	9
0000000A	00000001	410	R10	EQU	10
0000000B	00000001	411	R11	EQU	11
0000000C	00000001	412	R12	EQU	12
0000000D	00000001	413	R13	EQU	13
0000000E	00000001	414	R14	EQU	14
0000000F	00000001	415	R15	EQU	15

417 **END**

MACRO DEFN REFERENCES

No defined macros

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image Region CSECT	IMAGE	1724	000-6BB	000-6BB
		1724	000-6BB	000-6BB
	CU12TST	1724	000-6BB	000-6BB

STMT

FILE NAME

1

/devstor/dev/tests/. /CU12-01-xpage. asm

**** NO ERRORS FOUND ****